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EXAMINER	
MOORE JR, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,407	CHU, TAM-ANH	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,17-27 and 33-43* is/are rejected.

7)☒ Claim(s) *12-16,28-32 and 44-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1, 2, 8-11, 17, 18, 24-27, 33, 34, and 40-43** are rejected under 35 U.S.C. 102(e) as being anticipated by Sang et al. (U.S. 6,401,147) ("Sang"). Sang teaches all of the limitations of the specified claims with the reasoning that follows.

Regarding claim **1**, "a buffer memory of a first type to store data associated with a connection identifier corresponding to a channel in a network" is anticipated by input queue write side 410 (buffer memory of first type) of Figure 4 that receives and stores frame pointer entries (data) that point (associate) to buffers (connection identifier) in external memory as spoken of on column 10, line 66 – column 11, line 3.

"The data being organized into at least one chunk based on a linked list" is anticipated by the frame pointer data structure (linked list) shown in Figure 6A organized into queue write side 610 (chunk) and queue read side 612 (chunk) that are linked.

"The connection identifier identifying a connection in the channel" is anticipated by the buffers (connection identifier) in external memory that store (indicate) specific bytes of data frames as spoken of on column 11, lines 1-3.

"The data being part of a data stream associated with the connection" is anticipated by frame pointer entries (data) that point (associate) to buffers (connection) in external memory as spoken of on column 10, line 66 – column 11, line 3.

Lastly, "a packet memory of a second type coupled to the buffer memory to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory" is anticipated by external SSRAM memory block 36 (packet memory) of Figure 1 that receives burst writes of data from queue write side 410 (buffer memory) of Figure 4 via queue overflow storage area 414 as spoken of on column 11, lines 37-43.

Regarding claim **2**, "a descriptor memory to store descriptor information corresponding to the at least one chunk" is anticipated by queue overflow storage area 414 (descriptor memory) of Figure 4. Lastly, "a controller coupled to the descriptor memory and the buffer memory to control data transfer between the buffer memory and the packet memory using the descriptor information" is anticipated by queue overflow engine 416 (controller) of Figure 4 that determines whether to directly pass the pending entry to the queue read side 412 or to burst write the data to the overflow storage area 414 as spoken of on column 11, lines 8-26.

Regarding claims **8 and 40,** "an ingress queue to buffer the data stream of a packet from an ingress of the channel, the packet having a packet size" and "a queue segmenter to chunk the data stream into the at least one chunk" is anticipated by queue overflow engine 416 of Figure 4 that determines whether to directly pass the pending

entry from queue write side 410 (ingress) to the queue read side 412 or to burst write the data to the overflow storage area 414 as spoken of on column 11, lines 8-26.

Regarding claims **9 and 41,** "wherein the buffer memory comprises an input buffer memory to store the at least one chunk transferred from the queue segmenter" is anticipated by input queue write side 410 (input buffer memory) of Figure 4 that receives and stores frame pointer entries as spoken of on column 10, line 66 – column 11, line 3.

Regarding claims **10 and 42,** "wherein the input buffer memory comprises a queue associated with the connection identifier, the queue having a threshold and being configured to store the at least one chunk" is anticipated by the frame pointer data structure shown in Figure 6A organized into queue write side 610 (chunk) containing 64 13-bit entries 614.

Regarding claims **11 and 43,** "wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request" is anticipated by the overflow transfer mode between queue write side 410 and overflow storage area 414 spoken of on column 11, lines 23-26.

Regarding claim **17**, "storing data associated with a connection identifier corresponding to a channel in a network in a buffer memory of a first type" is anticipated by input queue write side 410 (buffer memory of first type) of Figure 4 that receives and stores frame pointer entries (data) that point (associate) to buffers (connection identifier) in external memory as spoken of on column 10, line 66 – column 11, line 3.

"The data being organized into at least one chunk based on a linked list" is anticipated by the frame pointer data structure (linked list) shown in Figure 6A organized into queue write side 610 (chunk) and queue read side 612 (chunk) that are linked.

"The connection identifier identifying a connection in the channel" is anticipated by the buffers (connection identifier) in external memory that store (indicate) specific bytes of data frames as spoken of on column 11, lines 1-3.

"The data being part of a data stream associated with the connection" is anticipated by frame pointer entries (data) that point (associate) to buffers (connection) in external memory as spoken of on column 10, line 66 – column 11, line 3.

Lastly, "providing access to the stored data using a packet memory of a second type when a transfer condition occurs, such that the data is transferred between the buffer memory and the packet memory" is anticipated by external SSRAM memory block 36 (packet memory) of Figure 1 that receives burst writes of data from queue write side 410 (buffer memory) of Figure 4 via queue overflow storage area 414 as spoken of on column 11, lines 37-43.

Regarding claim **18**, "storing descriptor information corresponding to the at least one chunk in a descriptor memory" is anticipated by queue overflow storage area 414 (descriptor memory) of Figure 4. Lastly, "controlling data transfer between the buffer memory and the packet memory using the descriptor information" is anticipated by queue overflow engine 416 of Figure 4 that determines whether to directly pass the pending entry to the queue read side 412 or to burst write the data to the overflow storage area 414 as spoken of on column 11, lines 8-26.

Regarding claim **24,** "buffering the data stream of a packet from an ingress of the channel by an ingress queue, the packet having a packet size, and segmenting the data stream into the at least one chunk" is anticipated by queue overflow engine 416 of Figure 4 that determines whether to directly pass the pending entry from queue write side 410 (ingress) to the queue read side 412 or to burst write the data to the overflow storage area 414 as spoken of on column 11, lines 8-26.

Regarding claim **25,** "storing the at least one chunk transferred from the queue segmenter in an input buffer memory" is anticipated by input queue write side 410 (input buffer memory) of Figure 4 that receives and stores frame pointer entries as spoken of on column 10, line 66 – column 11, line 3.

Regarding claim **26**, "storing the at least one chunk in queue associated with the connection identifier, the queue having a threshold" is anticipated by the frame pointer data structure shown in Figure 6A organized into queue write side 610 (chunk) containing 64 13-bit entries 614.

Regarding claim **27**, "wherein the transfer condition includes at least one of an overflow of the threshold, the packet size, and a scheduled egress request" is anticipated by the overflow transfer mode between queue write side 410 and overflow storage area 414 spoken of on column 11, lines 23-26.

Regarding claim **33**, "a channel in a network having an ingress and egress" is anticipated by the path (channel) shown in Figure 4 between queue write side 410 (ingress) and queue read side 412 (egress).

"A data buffer circuit coupled to the channel to buffer data transmitted over the channel" is anticipated by queue structure 400 (data buffer circuit) of Figure 4.

"An input buffer memory of a first type to store data associated with a connection identifier corresponding to the channel" is anticipated by input queue write side 410 (input buffer memory of first type) of Figure 4 that receives and stores frame pointer entries (data) that point (associate) to buffers (connection identifier) in external memory as spoken of on column 10, line 66 – column 11, line 3.

"The data being organized into at least one chunk based on a linked list" is anticipated by the frame pointer data structure (linked list) shown in Figure 6A organized into queue write side 610 (chunk) and queue read side 612 (chunk) that are linked.

"The connection identifier identifying a connection in the channel" is anticipated by the buffers (connection identifier) in external memory that store (indicate) specific bytes of data frames as spoken of on column 11, lines 1-3.

"The data being part of a data stream associated with the connection" is anticipated by frame pointer entries (data) that point (associate) to buffers (connection) in external memory as spoken of on column 10, line 66 – column 11, line 3.

"An output buffer memory of the first type to store the data transferred from the input buffer memory" is anticipated by output queue read side 412 (output buffer memory of first type) of Figure 4 that receives data entries either directly from queue write side 410 or queue overflow storage area 414 as spoken of on column 11, lines 8-26.

Lastly, "a packet memory of a second type coupled to the input and the output buffer memories to provide access to the stored data when a transfer condition occurs, such that the data may be transferred between the buffer memory and the packet memory" is anticipated by external SSRAM memory block 36 (packet memory) of Figure 1 that receives burst writes of data from queue write side 410 (buffer memory) of Figure 4 via queue overflow storage area 414 as spoken of on column 11, lines 37-43.

Regarding claim **34**, "a descriptor memory to store descriptor information corresponding to the at least one chunk" is anticipated by queue overflow storage area 414 (descriptor memory) of Figure 4. Lastly, "a controller coupled to the descriptor memory and the input and output buffer memories to control data transfer between the buffer memories and the packet memory using the descriptor information" is anticipated by queue overflow engine 416 (controller) of Figure 4 that determines whether to directly pass the pending entry to the queue read side 412 or to burst write the data to the overflow storage area 414 as spoken of on column 11, lines 8-26.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **3-7, 19-23, and 35-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sang et al. (U.S. 6,401,147) ("Sang") in view of Herring et al. (U.S. 6,542,502) ("Herring").

Regarding claims **3, 19, and 35,** Sang teaches the apparatus of claim **2**, the method of claim **18**, and the system of claim **34**, respectively. Sang fails to explicitly teach storing chunk information associated with the linked list in a chunk header. However, Herring teaches a next chunk field 304 (chunk header) associated with the data field of a chunk as shown in Figure 3. This field indicates the next chunk in the linked list. At the time of the invention, it would have been obvious to someone skilled in the art to combine the chunk header field of Herring with the teachings of Sang in order to provide a way to order the packets within each packet queue as spoken of on column 3, lines 6-22 of Herring.

Regarding claims **4, 20, and 36,** Sang further teaches frame pointer entries that point to buffers in external memory (other chunk) as spoken of on column 10, line 66 – column 11, line 3.

Regarding claims **5, 21, and 37,** Sang further teaches frame pointer entries that point to a first buffer in external memory (head chunk) as spoken of on column 10, line 66 – column 11, line 3.

Regarding claims **6, 22, and 38,** Sang further teaches queue overflow storage area 414 (descriptor memory) of Figure 4 that stores frame pointers that point to buffers in external memory (head and tail chunks) as spoken of on column 10, line 66 – column 11, line 3.

Regarding claims **7, 23, and 39,** Sang further teaches buffers (connection identifier) in external memory that store (indicate) specific bytes of data frames as spoken of on column 11, lines 1-3.

Allowable Subject Matter

5. Claims **12-16, 28-32, and 44-48** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim **12**, Sang teaches the apparatus of claim **11**. Sang fails to teach a data combiner for combining the data portions of different chunks and burst writing to either the packet memory or to an output buffer memory based on the packet size.

Regarding claims **13-16**, these claims are further limiting to claim **12** and are thus also allowable over the prior art of record.

Regarding claim **28**, Sang teaches the method of claim **27**. Sang fails to teach combining the data portions of different chunks and burst writing to either the packet memory or to an output buffer memory based on the packet size.

Regarding claims **29-32**, these claims are further limiting to claim **28** and are thus also allowable over the prior art of record.

Regarding claim **44**, Sang teaches the system of claim **43**. Sang fails to teach a data combiner for combining the data portions of different chunks and burst writing to either the packet memory or to an output buffer memory based on the packet size.

Regarding claim **45**, Sang teaches the system of claim **42**. Sang fails to teach an ordered list of pointers associated with the chunk headers that is transferred to the output buffer memory at a location pointed to by the head pointer as well a read circuit

to burst transfer the contiguous data block from the packet memory to the output buffer memory using the ordered list of pointers.

Regarding claims **46-48**, these claims are further limiting to claim **45** and are thus also allowable over the prior art of record.

Response to Arguments

7. Applicant's arguments with respect to amended claims **1-11, 17-27, and 33-43** have been considered but are moot in view of the new ground(s) of rejection provided above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (571) 272-3168. The examiner can normally be reached on Monday-Friday (8:30am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael J. Moore, Jr.
Examiner
Art Unit 2666

mjm MM

DUNG TON
PRIMARY EXAMINER